

WHAT IS CLAIMED IS:

1.    A method of operating a first-in first-out (FIFO)  
5    pointer circuit comprising:

        coupling a plurality of shift registers in a circular  
fashion; and

        applying a rising edge and a falling edge of a pointer  
clock signal to clock inputs of the plurality of shift  
10    registers in an alternating fashion.

2.    A method of operating a first-in first-out (FIFO)  
pointer circuit comprising:

        coupling a plurality of shift registers in a circular  
15    fashion;

        applying the same one of a rising edge or a falling edge  
of a pointer clock signal to clock inputs of the plurality of  
shift registers in a full rate mode of operation; and

        applying the rising edge and the falling edge of the  
20    pointer clock signal to clock inputs of the plurality of shift  
registers in an alternating fashion in a half rate mode of  
operation.

3.    A first-in-first-out (FIFO) pointer reset circuit  
25    comprising:

        a clock present detector coupled to receive a read clock  
and a write clock and configured to generate a CKPRES signal  
indicating status of the write clock; and

        logic circuit coupled to receive a first reset signal,  
30    the CKPRES signal, the write clock and the read clock, and  
configured to generate a write pointer reset signal and a read  
pointer reset signal in response thereto.

4.    The FIFO pointer reset circuit of claim 3 wherein  
the logic circuit further receives a lock detect signal  
5    indicating a phase status of the read clock, the lock detect  
signal being logically combined with other input signals to  
the logic circuit.

5.    The FIFO pointer reset circuit of claim 3 wherein  
10   the logic circuit comprises:

     a first flip-flop having a reset input coupled to receive  
a second reset signal, a clock input coupled to receive the  
read clock, and an output; and

     a second flip-flop having a data input coupled to the  
15   output of the first flip-flop, a reset input coupled to  
receive the second reset signal, a clock input coupled to  
receive the read clock and an output coupled to generate the  
read pointer reset signal.

6.    The FIFO pointer reset circuit of claim 5 wherein  
20   the logic circuit further comprises:

     a third flip-flop having a reset input coupled to receive  
the second reset signal, a clock input coupled to receive the  
write clock, and an output; and

25       a fourth flip-flop having a data input coupled to the  
output of the third flip-flop, a reset input coupled to  
receive the second reset signal, a clock input coupled to  
receive the write clock and an output coupled to generate the  
write pointer reset signal.

30       7.    The FIFO pointer reset circuit of claim 6 wherein  
data input of the first flip-flop and a data input of the  
second flip-flop couple together and to a third reset signal.

5        8.    The FIFO pointer reset circuit of claim 7 wherein  
the logic circuit further comprises a fifth flip-flop having a  
data input coupled to the first reset signal, a clock input  
coupled to the write clock, a reset input coupled to the  
second reset signal, and an output coupled to generate the  
third reset signal.

10       9.    The FIFO pointer reset circuit of claim 6 wherein  
the logic circuit further comprises logic gates that combine  
the CKPRES signal with a lock detect signal that indicates a  
phase status of the read clock, and generate the second reset  
signal.

15       10.   The FIFO pointer reset circuit of claim 6 further  
comprising a first multiplexer having a first input coupled to  
receive the read clock, a second input coupled to receive a  
second read clock having a frequency that is different than  
20       that of the read clock, a select input, and an output coupled  
to an input of the clock present detector, wherein a control  
signal applied to the select input selects one of either the  
read clock or the second read clock to be applied to the clock  
present detector.

25       11.   The FIFO pointer reset circuit of claim 10 wherein  
the frequency of the second read clock is half that of the  
read clock.

30       12.   The FIFO pointer reset circuit of claim 11 wherein  
the logic circuitry further comprises a second multiplexer  
having a first input coupled to the write clock, a second  
input coupled to an inverted version of the write clock, a

select input, and an output coupled to the clock input of the third flip-flop.

5            13. The FIFO reset pointer circuit of claim 6 wherein the logic circuitry further comprises a selectable flip-flop that is selectably coupled in series with the first flip-flop, the selectable flip-flop having a reset input coupled to the  
10 second reset signal and a clock input coupled to receive the read clock.

14. A method of resetting first-in first-out (FIFO) pointer circuits comprising:

15            detecting the presence of a FIFO write clock signal and generating a CKPRES signal in response thereto;

             detecting the lock status of a FIFO read clock signal phase-locked loop and generating a LCKDET signal in response thereto;

20            receiving a reset signal; and

             logically combining the CKPRES, the LCKDET and the reset signal to reset the FIFO pointer circuits when the write clock signal is lost, or when the read clock is not locked, or when the reset signal is asserted.

25            15. The method of claim 14 wherein the step of logically combining further comprises resetting a pair of serially-coupled flip-flops that are clocked by the FIFO read clock.

30            16. A write clock present detector for a first-in first-out (FIFO) circuit, the write clock present detector comprising:

a read shift register having a first plurality of  
 serially-coupled registers and configured to shift a read flag  
 5      signal in response to a read clock;

        a write shift register having a second plurality of  
 serially-coupled registers and configured to shift a write  
 flag signal in response to a write clock; and

        a logic circuit coupled to an output of the read shift  
 10     register and an output of the write shift register, and  
 configured to logically combine the write flag signal with the  
 read flag signal to generate a write clock present detect  
 output signal.

15           17. The write clock present detector of claim 16 wherein  
 the first plurality of registers in the read shift register is  
 larger in number compared to the second plurality of registers  
 in the write shift register.

20           18. The write clock present detector of claim 17 wherein  
 the registers in the write shift register and the registers in  
 the read shift register are resettable registers with each  
 having a reset input.

25           19. The write clock present detector of claim 18 wherein  
 the logic circuit comprises a reset circuit having an input  
 coupled to an output of the read shift register, and an output  
 coupled to the reset input of each of the registers in the  
 read and the write shift registers.

30           20. The write clock present detector of claim 19 wherein  
 the reset circuit comprises a serially-coupled pair of flip-  
 flops coupled to an output of the read shift register and a  
 logic gate having inputs coupled to outputs of the pair of  
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flip-flops and an output coupled to the output of the reset circuit.

5            21. The write clock present detector claim 17 wherein the write shift register comprises N registers and the read shift register comprises N+3 registers.

10           22. The write clock present detector of claim 21 wherein the logic circuit comprises:

          a logic gate coupled to receive an output of the N<sup>th</sup> write register and an output of the N<sup>th</sup> read register and to generate a DET output signal; and

15           a flip-flop having a data input coupled to receive the DET output signal, a clock input coupled to the (N+3)<sup>th</sup> output of the read register, and an output coupled to generate a write clock present detect signal.

20           23. A method of detecting the presence of a write clock for a first-in first-out (FIFO) circuit, the method comprising:

          propagating a read flag signal through a read shift register in response to a read clock;

25           propagating a write flag signal through a write shift register in response to the write clock; and

          comparing an output of the read shift register with an output of the write shift register to generate a write clock present output signal.

30           24. The method of claim 23 further comprising periodically resetting the read shift register and the write shift register.

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25. A first-in first-out (FIFO) pointer circuit comprising:

5        a serial chain of N registers coupled in circle and configured to shift a pointer signal in response to a pointer clock; and

10       a pointer abnormality detector having a logic circuit with N inputs respectively coupled to N outputs of the N registers,

wherein, the logic circuit is configured to detect lack of the pointer signal or presence of multiple pointer signals.

15       26. The FIFO pointer circuit of claim 25 wherein the logic circuit in the pointer abnormality detector comprises a first logic gate having N-1 inputs coupled to N-1 outputs of the N registers and an output, and a second logic gate having a first input coupled to the output of the first logic gate and a second input coupled to one output of the N registers  
20       that is not coupled to the first logic gate.

25       27. The FIFO pointer circuit of claim 26 wherein the logic circuit further comprises a flip-flop having a data input coupled to an output of the second logic gate, a clock input and an output.

30       28. The FIFO pointer circuit of claim 26 wherein the first logic gate is an OR gate, and the second logic gate is an exclusive NOR gate.

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